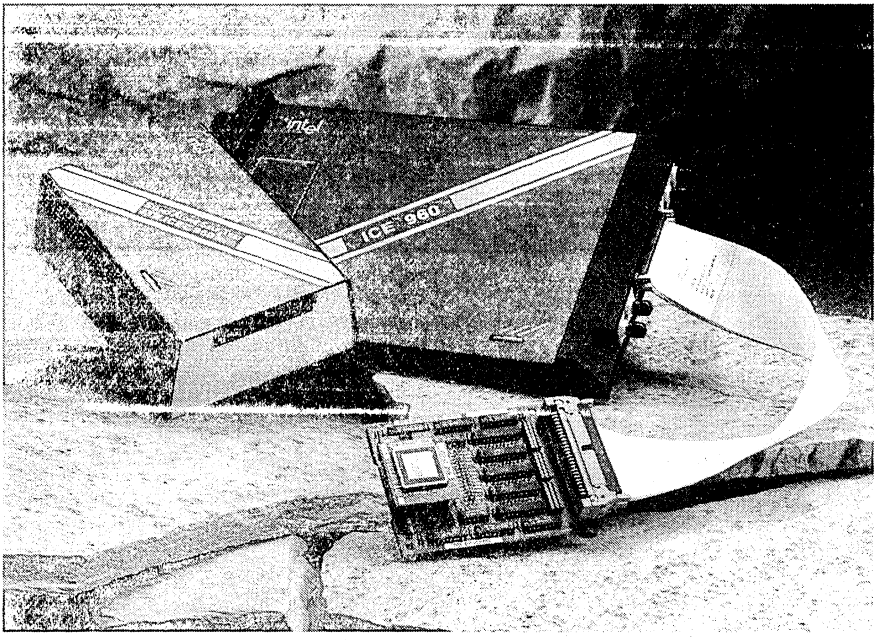
ICE™-960SB AND ICE-960KB IN-CIRCUIT EMULATOR



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INTERCHANGEABLE PROBES

The ICE™-960 in-circuit emulator delivers real-time hardware and software debugging capabilities for i960™ SA/SB and i960 KA/KB-based designs. Features include full-speed emulation of each of the microprocessors, powerful breakpoint specification, fastbreaks, optional relocatable expansion memory, two types of trace capability, large trace buffering, sophisticated human interface and high-speed communication links with the DOS host. The ICE-960 in-circuit emulator gives you unmatched control over all phases of hardware/software debug, including developing, integrating and testing, which improves development productivity and improves time to market.

FEATURES

- Real-Time Emulation of the i960 KA/KB microprocessors up to 25 MHz and emulation of the i960 SA/SB to 16 MHz
- Full symbolic integration with Intel ASM and C compilers
- Optional ICE960KBREM/ ICE960SBREM boards provide 2 Mbytes of ICE memory which can overlay user ROM or RAM.
- Examine and modify memory and the i960 registers
- Dynamically monitor and update program variables via fastbreaks
- Breakpoint capabilities include: execution address, instruction type, bus read/write/access, and data value. Qualification of events is based on an occurrence counter and an 8-state states-machine

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FEATURES

- Hosted on IBM PC AT* or compatible and supporting RS232, RS422 and Ethernet operation
- 1024 frame trace buffer for execution and/or bus trace and time tags
- The on-chip cache does not effect collection of the execution trace
- 256 Kbytes of memory in standalone self-test (SAST) unit
- Real-time bus trace with time-tags for tracking code execution time
- Assembly and disassembly of code in i960 instruction mnemonics
- ICE to component interconnect includes support for surface-mounted and socketed 84-pin PLCCD and surface mounted 80-pin EIAJ QFP i960 SA/SB and 132-pin PGA for i960 KA/KB

The ICE-960 in-circuit emulator provides emulation of the i960 SA/SB at speeds to 16 MHz and the i960 KA/KB at speeds to 25 MHz, thus providing early detection of subtle timing problems that may arise at full speed. Intel's intimate knowledge of the component makes possible the tightest conceivable conformance between timing parameters of the emulator and the target microprocessor.

PROCESSOR/MEMORY EXAMINATION AND MODIFICATION

The i960 registers can be accessed mnemonically (e.g. g12, r5, fp3) with the ICE-960 emulator software. Data can be displayed or modified in hexadecimal, decimal, octal, or binary and by data type (byte, word, etc). Program memory contents can be modified as i960 assembly instruction mnemonics.

PROGRAM TRACING

The ICE-960 emulator can store 1024 frames of program execution history processor/address/data bus activity in the trace buffer. Each frame of program execution contains a discontinuity address (branch, call, return, etc) and a time-tag. This information can be used to reconstruct a history of the program execution. With the execution trace option enabled, the ICE-960 will run at less than full speed. Each trace frame of bus cycles contains one complete bus burst trace. Collection of trace information is controlled by a logic analyzer type moving trace window and by bus access type.

EVENT RECOGNITION (BREAKPOINT CONTROL) AND EMULATION CONTROL

ICE-960 provides comprehensive event recognition capabilities including: two hardware and thirty-two software breakpoints for instruction execution breakpoints, and use of the internal debug registers to recognize execution of certain instruction types such as branch or call instructions. Bus analysis logic provides recognition of external bus addresses qualified by read, write, or access type as well as data values. The data values may be entered as masked values and qualified by type. Two synchronization lines are provided for recognition of external events. ICE-960 also provides qualification of events based on an occurrence counter or by a recognition sequence of up to 8 events. Additionally, emulation can be automatically stopped when the trace buffer is full. Besides the ability to execute program code at full speed between specified points, the ICE-960 emulator provides the capability to single-step through program code.

RELOCATABLE EXPANSION MEMORY

An optional board provides ICE-960 with 2 Mbytes of relocatable expansion memory which allows users to develop applications either before the target system memory is working, or in place of ROM or EPROM to speed the debugging cycle. This memory can be mapped in two separate 1 Mbyte partitions on 1 Mbyte boundaries.

For the new ICE960KBREM board, the memory waitstate pattern is (3,1,1,1) when the users system does not return RDY# for accesses in the mapped area. For accesses where the user system does return RDY# for these areas, the waitstate pattern will be the larger of (3,1,1,1) or user waitstate pattern plus (2,2,2,2). For either board, the size and shape of the board is identical to the ICE probe and is installed between the probe and the user's target system when in use. The memory configuration can be mapped via an ICE MAP command.

The ICE960KBREM/ICE960SBREM cards add some constraints when used with the ICE in a users target system. First, users should qualify bus drivers/buffers with DEN# in order to eliminate potential bus conflict between the REM board and their target memory while

using the ICE. Second, the 1M Byte partition size can not be reduced and may effect the design of the users memory subsystem. Third, the REM boards delay the ADS# and DEN# signals by 5 ns (typical) and delays the RDY# signal by 4 ns (typical). Fourth, it adds loading, capacitance, and power requirements as shown in tables 3 and 4.

STANDALONE OPERATION

Product software can be developed and debugged prior to and independent of hardware availability with the Standalone Self Test unit (SAST), which contains 256 Kbytes of two wait-state program memory. The SAST also provides diagnostic testing to assure full functionality of the ICE-960 emulator.

VERSATILE AND POWERFUL HOST SOFTWARE

ICE-960 provides an easy-to-use human interface which utilizes color forms to complement a powerful command set. The software includes: an on-line help facility, a dynamic command entry and syntax guide, screen oriented editor, assembler and disassembler, input/output redirection, command piping, DOS command entry, and the ability to customize the command set via debug procedures and literal definitions.

DEBUG PROCEDURES AND LITERALS

Debug procedures (PROCs) are user-defined groups of ICE960 emulator commands. They can be stored on disk and recalled during later debugging sessions. PROCs can be used to simplify the process of debugging by grouping repetitive emulator commands, which can then be accessed by typing the name of the PROC. Literals are user-defined abbreviations for whole or partial ICE-960 emulator commands. Literals are a shorthand method of customizing the emulator commands to fit your needs and preferences.

ICE TO COMPONENT INTERCONNECT SYSTEM

Using the On-Circuit Emulation (ONCE) i960 SA/SB silicon feature, ICE960SB can be used in systems with surface-mounted i960 SA/SB components in either PLCC or EIAJ QFP packages. The hinge cable adapters included in the various ICE kits and pictured to the right, are placed directly on top of the surface mounted i960 SA/SB device. The circuitry necessary for the emulator to take control from the target processor is fully supported in the emulator. No additional circuitry is required.

Of course, socketed support for i960 SA/SB components in PLCC packages, or i960 KA/KB components in PGA packages are also supported. Please see Figures 1, 2, 3, and 4 for ICE Probe physical characteristics. Refer to Table 5 for hinge cable loading and delay characteristics.

WORLDWIDE SERVICE, SUPPORT, AND TRAINING

To augment its development tools, Intel offers a full array of seminars, classes, workshops, field application engineering expertise, hotline technical support, and on-site service.

Intel also offers a Software Support contract which includes technical software information, automatic distributions of software and documentation updates, *iCOMMENTS* publication, remote diagnostic software, and a development tools troubleshooting guide.

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FEATURES

HIGH-SPEED HOST-TO-ICE COMMUNICATIONS PROTOCOLS

ICE-960 supports RS232 and RS422 communications protocols to 115 KBaud and 1152 KBaud respectively depending upon the ability of the host to support the specific rate. Testing for these systems and the configurations involved are described in the following sections.

Intel's 90-day Hardware Support package includes technical hardware information, warranty on parts, labor, material, and on-site hardware support.

Intel Development Tools also offers a 30-day, money-back guarantee to customers who are not satisfied after purchasing any Intel development tool.

SPECIFICATIONS

HOST REQUIREMENTS

IBM PC-AT (minimum requirements) with 640 KBytes of conventional memory

1 MByte of RAM (Lotus, Intel, Microsoft expanded memory specification)

20 MByte Fixed Disk

At least one 5¼" or 3½" Floppy Disk drive

RS232 or RS422 Communication Interface

DOS Operating System (version 3.2 or 3.3)

TESTED HOST CONFIGURATIONS

IBM PC-AT with DOS 3.3. Tested with built-in RS232 and a Quatech DS202 Asynchronous RS422 Communications Board with 16550 Option

COMPAQ Deskpro 386* with DOS 3.3. Tested with built-in RS232 and Quatech DS202 Asynchronous RS422 Communications Board with 16550 Option

Systems Based on an Intel 301/302™ Box with DOS 3.3. Tested with built-in RS232 to 115.2 KBaud and a Quatech DS202 Asynchronous RS422 Communications Board with 16550 Option to 1.152 MBaud

IBM Personal System/2* with DOS 4.01. Tested with built-in RS232

REQUIRED SYSTEM RESOURCES

The ICE-960 emulator requires the following: a) exclusive use of the i960 SA/SB or i960 KA/KB's on-chip debug registers and b) a minimum of 256 bytes of target system RAM used to flush the i960 local registers.

MECHANICAL SPECIFICATIONS

TABLE 1. ICE-960 Emulator Physical Characteristics

Unit	Width		Height		Length		Weight	
	Inches	cm	Inches	cm	Inches	cm	lbs	kg
Control Unit	10.5	26.7	1.5	3.8	16.0	40.6	6.0	2.72
Processor Module*	3.8	9.6	1.5	3.8	5.0	12.7		
SAST	6.0	15.2	2.0	5.1	8.0	20.3	3.5	1.59
OIB	3.8	9.6	0.9	2.3	5.1	13.0		
Power Supply	2.8	7.1	4.2	10.7	11.0	27.9	4.7	2.14
User Cable					22.0	55.9		
Serial Cables					12.0'	3.66m		

*Measurement includes target adaptor

SPECIFICATIONS

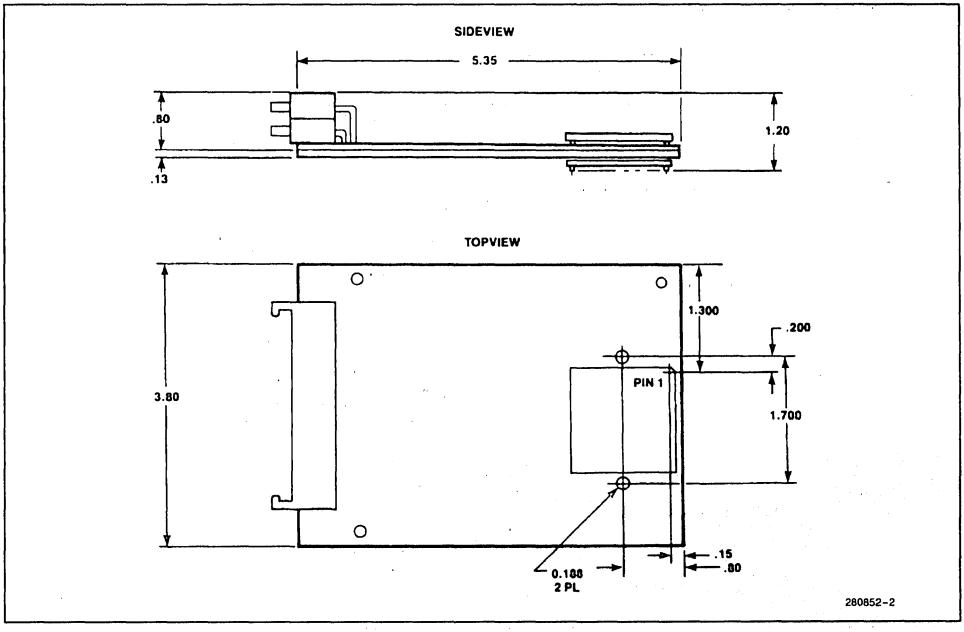

Figure 1: ICE960KB25 Processor Module

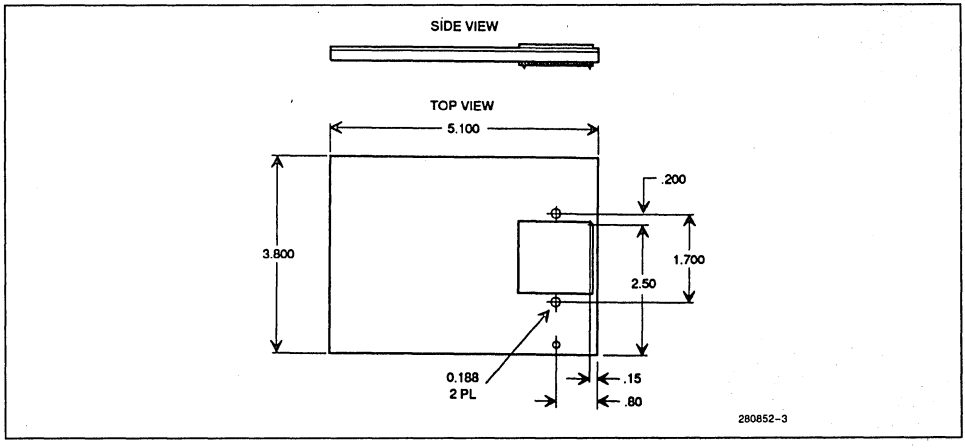

Figure 2: Optional Isolation Board

SPECIFICATIONS

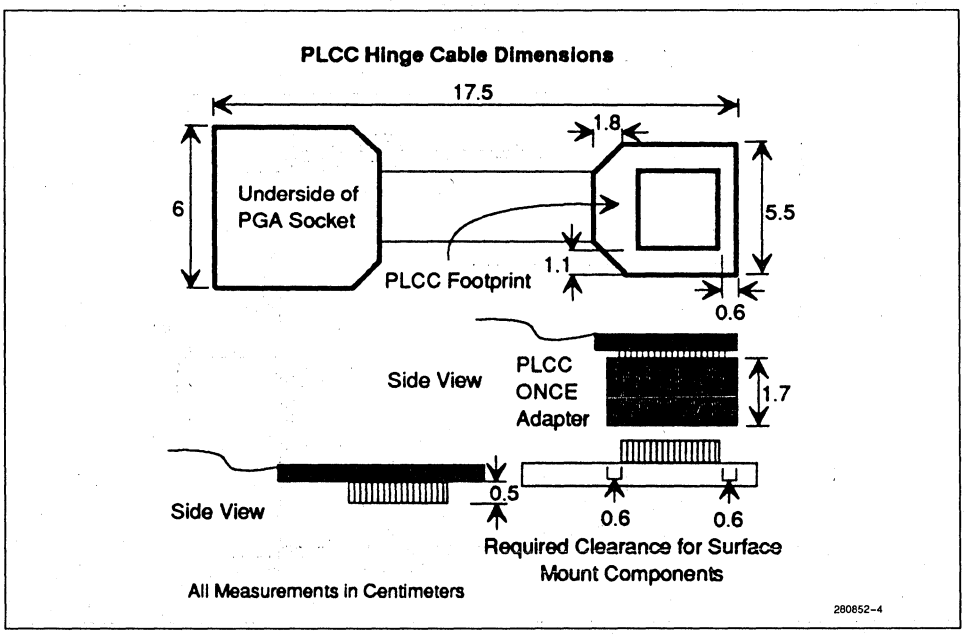

Figure 3: ICE960SB16C Adapter

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

SYNC Line Specification

The SYNCIN line must be valid for at least one instruction cycle because it is only sampled on bus access boundaries. The SYNCIN line is a standard TTL input. The SYNCOUT line is driven by a TTL open collector with a 4.75 KΩ pull-up resistor

AC/DC Specifications

The Optional Isolation Board (OIB) isolates the ICE-960 probe from an untested user target system. When the OIB is in use, the ICE-960 AC and DC specifications differ from the i960 microprocessor as shown below. When the OIB is not installed, the ICE-960KB timing specifications are identical to those of the i960 component.

TABLE 2. AC Specifications with the OIB Installed

Symbol*	Parameter	16 MHz 80960SB		25 MHz 80960KB	
		Min	Max	Min	Max
T1	Clock Period	32 ns	125 ns	20 ns	125 ns
T2	Clock Low Time	9 ns		6 ns	
T3	Clock High Time	9 ns		6 ns	
T4	Clock Fall Time		10 ns		10 ns
T5	Clock Rise		10 ns		10 ns
T6	Output Valid Delay A(2:3), BE#(0:1), BLAST#,* DEN#, DTR#, WR#** A/D Lines***		 40 ns 40 ns		 33 ns 33 ns
T6 AS	AS Valid Delay (AS#)		36 ns		33 ns
T7	ALE# Width	16 ns		12 ns	
T8	ALE# Valid Delay		36 ns		33 ns
T9	Output Float Delay A(2:3), BE#(0:1), BLAST#,* DEN#, DTR#, WR#** A/D Lines		 50 ns 50 ns		 35 ns 40 ns
T10	Input Setup 1 HLDA, INT0#, INT1, INT2, INT3#	 13 ns		 6 ns	
T11	Input Hold HLDA, INT0#, INT1, INT2, INT3# HOLD, READY#, LOCK#	 10 ns 10 ns		 13 ns 13 ns	
T12	Input Setup 2 HOLD, READY#, LOCK#	 17 ns		 11 ns	
T13	Setup to ALE# Inactive	7 ns		7 ns	
T14	Hold after ALE#	5 ns		5 ns	
T15	RESET# Hold	4 ns		4 ns	
T16	RESET# Setup	4 ns		4 ns	
T17	RESET# Width	1281 ns		820 ns	

*T_{PLH} dependent on termination for KB control signals
**OIB does not float A/D bus during T_r and T_i (between bus cycles)
***Output Valid Delay for control signals after HOLD ACKNOWLEDGE is deasserted 50 ns for 80960SB and 43 ns for 80960KB

SPECIFICATIONS

TABLE 3. ICE-960 Emulator DC Specifications

	ICE Probe	OIB	REM	Processor Speed
ICE960SB	1.4	0.4	0.5	16
ICE960KB	1.4	0.6	0.7	25

TARGET SYSTEM DESIGN CONSIDERATIONS

In addition to the mechanical, power consumption, and signal loading considerations for the ICE probe, the following points should be taken into account when the target system is being designed:

1) [SA/SB/KA/KB/MC]

   The AD bus should not be driven by an external source unless DEN# is asserted.

2) [SA/SB/KA/KB/MC]

   The LOCK# signal must be terminated as recommended in the 80960SA/SB component data sheet.

3) [SA/SB/KA/KB/MC]

   To guarantee timings, the ICE requires ±5% supply voltage to the target system (i.e., ICE probe power).

4) [SA/SB]

   To ensure correct bus trace the ICE requires a data hold time (T11) of 4 ns.

5) [SA/SB/KA/KB/MC]

   Each V_{CC} and GND pin of the processor must be connected to the appropriate voltage or ground and externally strapped close to the package.

6) [SA/SB/KA/KB/MC]

   Processor no connect (N.C.) pins must be left disconnected.

SPECIFICATIONS

TABLE 4. Additional DC Loading

Signal	(ICE Probe)		(OIB)		(KB REM)		(SB REM)	
	I_{IH} Max	I_{IL} Max	I_{IH} Max	I_{IL} Max	I_{IH} Max	I_{IL} Max	I_{IH} Max	I_{IL} Max
AD(0:31)	25 µA	25 µA	15 µA	−15 µA	120 µA	0.7 mA	20 µA	100 µA
ADS#	25 µA	25 µA	115 µA	−15 µA	Driven by 74AS760 w/ 4.7k Pull-Up		10 µA	10 µA
DEN#	25 µA	25 µA	115 µA	−15 µA				
W/R#	25 µA	25 µA	115 µA	−15 µA	150 µA	1.7 mA	10 µA	10 µA
CLK2	50 µA	500 µA	25 µA	−25 µA	130 µA	2.9 mA	20 µA	1600 µA
RESET	25 µA	250 µA	45 µA	−750 µA	250 µA	0.3 mA	10 µA	10 µA
BE(0:3)#	25 µA	25 µA	115 µA	−15 µA	10 µA	0.1 mA	10 µA	10 µA
READY#	25 µA	25 µA	45 µA	−750 µA	750 µA	0.8 mA	25 µA	260 µA
ALE#	25 µA	25 µA	15 µA	−15 µA	20 µA	0.5 mA	10 µA	1600 µA
DT/R#	25 µA	25 µA	115 µA	−15 µA				
INT(0:3)	25 µA	25 µA	15 µA	−565 µA				
BADAC#	25 µA	25 µA	15 µA	−565 µA				
LOCK#	25 µA	25 µA	140 µA	−500 µA				
HOLD	25 µA	25 µA	45 µA	−750 µA				
FAILURE#	25 µA	25 µA	20 µA	−1 mA				

TABLE 5. 80960SB PLCC Hinge Cable Loading and Delay

Signal Loading	15 pF Typical
Signal Delay	Signals from Processor delayed 4 ns typical, Setup and Hold Timings unaffected.

ORDERING INFORMATION

Order Code	Description
ADPT80EIAJ	Hinge Cable Adapter for surface-mount i960SB EIAJ QFP packages. This adapter is included in the ICE960SB16J kit.
ADPT84PLCC	Hinge Cable Adapter for surface-mount and socketed i960SB PLCC packages. This adapter is included in the ICE960SB16C kit.
ICE960SB16C	ICE960 base, i960 SA/SB probe, 84-pin PLCC surface-mount and socketed target component interconnect, and RS232 and RS422 communication cables. (Shrink-Wrap license, Class 1)
ICE960SB16J	ICE960 base, i960 SA/SB probe, 80-pin EIAJ surface-mount target component interconnect, and RS232 and RS422 communication cables. (Shrink-Wrap license, Class 1)
ICE960KB25	ICE960 base, i960 KA/KB probe, 132-pin PGA target component interconnect, and RS232 and RS422 communication cables. (Shrink-Wrap license, Class 1)
ICE960SBREM	Optional 2 MByte Relocatable Expansion Memory Board for i960 SA/SB components.
ICE960KBREM	Optional 2 MByte Relocatable Expansion Memory Board for 80960KA/KB components.
PTOI960SB16	Probe and Software to convert ICE960KB25 to ICE960SB16. An ADPT80EIAJ or ADPT84PLCC adapter kit should also be ordered with this package to support the component packaging type of your choice. (Shrink-Wrap license, Class 1)
PTOI960KB25	Probe and Software to convert ICE960SB16C or ICE960SB16J to ICE960KB25. (Shrink-Wrap license, Class 1)